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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/073,948	RHOADES ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-13,16,17,19-22,32,34,35,38,40,41,44,46,47,50,52,53,56 and 59-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-4,6-9,11-13,16,17,19-22,32,34,35,38,40,41,44,46,47,50,52,53,56 and 59-64.

DETAILED ACTION

1. Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are pending in this office action and presented for examination. Claims 1, 3, 7, 9, 11, 17, 20, 34-35, 28, 40-41, 44, 46-47, 50, 52-53, 56, 60-61, and 63-64 have been newly amended by amendment filed 6/25/2009.

2. The supplemental amendment filed 6/25/2009 has been entered and considered.

Claim Objections

3. Claims 22 and 46 are objected to because of the following informalities. Appropriate correction is required.

a. Claims 22 and 46 appear to be identical; one of these two claims should presumably be deleted.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "wherein the input device is operable to distribute data packets of unpredictable size in batches across said processing elements" in lines 6-7. It is indefinite as to whether "batches" in the claim refers to the data packets, or that which the data packets are distributed into.

b. Claims 2-4, 6-9, 11-13, 16-17, 19-22, 32, 34-35, 38, 40-41, 44, 46-47, 50, 52-53, 56, and 59-64 are rejected for failing to alleviate the rejection of claim 1 above.

7. Claim 7 recites the limitation "the processing elements are operable to control the input device." However, it is indefinite as to what this limitation is trying to convey, as examiner has perused the instant specification and it appears that it is not the processing elements which control the input device, but the thread sequence controller. See, for example, page 33, which discloses "[a] single hardware multi-threaded Thread Sequence Controller manages the issuing of instructions to the P/E array and the I/O engines" wherein the TSC is separate from the processing elements in Figure 4. As another example, see page 52, which discloses that a packet loading thread performs the scheduling of the transfer of packet data from the Distributor into the local memory of the PEs in the processor.

c. Claim 8 is rejected for failing to alleviate the rejection of claim 7 above.

8. Claim 9 recites the limitation "the processing elements are operable to control an output device." However, it is indefinite as to what this limitation is trying to convey, as

examiner has perused the instant specification and it appears that it is not the processing elements which control the output device, but the thread sequence controller. See, for example, page 33, which discloses "[a] single hardware multi-threaded Thread Sequence Controller manages the issuing of instructions to the P/E array and the I/O engines" wherein the TSC is separate from the processing elements in Figure 4. As another example, see page 52, which discloses that a packet unloading thread schedules the transfer of packet data from the local memory of PEs in the processor to the Collector.

9. Claim 11 recites the limitation "said input devices" and "said output devices" in line 2. However, there does not appear to be antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-4, 6-9, 11, 16-17, 20-21, 32, 40, 44, 52, 56, 59-60, and 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan et al. (Marsan)

(Router Architectures Exploiting Input-Queued, Cell-Based Switching Fabrics in view of Clauberg (WO 97/29613)

12. Consider claim 1, Marsan discloses an input device for receiving an incoming stream of data packets of unpredictable size (page 2, first indented paragraph, input IP datagrams are internally segmented into ATM-like cells); to process data received thereby (page 2, first indented paragraph, internally operates on fixed-size data units called cells);

However, Marsan does not disclose of the manner in which the cells are operated on, and thus does not disclose that a plurality of processing elements processes the data, and the input device is operable to distribute data packets of unpredictable size in batches across said processing elements such that the number of said processing elements across which each data packet is distributed is dynamically determined based at least in part on the size of the data packet; a data packet greater than a predetermined size being divided into portions and each portion distributed to a respective processing element; and a data packet less than a predetermined size being distributed to a single processing element; wherein the data processing architecture is operable to process at least one data packet at a time.

On the other hand, Clauberg discloses that a plurality of processing elements processes the data (Figure 1, for example; incoming data is processed by 14.1 to 14.5 and 15.1 to 15.5) and the input device is operable to distribute cells across one or more of said processing elements wherein the data processing architecture is operable to process at least one data packet at a time (Figure 1 as above; incoming cells are

processed in parallel and simultaneously within a processing path; demux 12 serves as the distributor of cells).

Clauberg's teaching results in very fast on-the-fly processing of fixed length cells even at very high data transmission rates (Clauberg, page 2, line 31 through page 3, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Clauberg with the invention Marsan in order to achieve very fast on-the-fly processing of fixed length cells even at very high data transmission rates. Note that Clauberg's teaching wherein cells are processed in parallel, when applied to the invention of Marsan wherein packets are divided into cells prior to processing, teach the overall limitations wherein whole data packets of unpredictable size are distributed among one or more of said processing elements such that the number of said processing elements across which each whole data packet is distributed is dynamically determined based at least in part on the size of the whole data packet, a data packet greater than a predetermined size being divided into portions and each portion distributed to a respective processing element; and a data packet less than a predetermined size being distributed to a single processing element (the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations).

13. Consider claim 2, Clauberg discloses the processing elements are arranged in a single instruction multiple data (SIMD) array (see Figure 1 for example, many processing elements performing the same operation on different data).

14. Consider claim 3, Marsan as modified by Clauberg discloses a data packet is allocated to as many processing elements as are necessary to store said packet and to process said packet (see the combination of the independent claim; the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations).

15. Consider claim 4, Marsan and Clauberg discloses the portions are of a fixed size (Marsan, page 2, first indented paragraph, fixed-size data units called cells; Clauberg, page 5, line 16 for example, fixed length cells).

16. Consider claim 6, Marsan as modified by Clauberg discloses the input device is operable to transfer data packets to the processing elements such that not all processing elements receive data (see the combination of the independent claim; the size of a variable length packet determines how many fixed length cells it is broken up into, and the cells are distributed to the processing elements regardless of packet considerations; a smaller packet would not be broken up into enough fixed length cells to send cells to all processing elements).

17. Consider claim 7, Marsan or Clauberg discloses the processing elements are operable to control the transfer of packet portions to the processing elements from the input device (an input device can be thought to collectively include the processing elements. Alternatively, Clauberg discloses of using a counter in page 10, line 7, which may be considered as part of the processing elements).

18. Consider claim 8, Marsan or Clauberg discloses the processing elements are operable to control the input device by means of software (it would have been obvious to one of ordinary skill in the art at the time of the invention that software can perform a function of hardware with more flexibility).

19. Consider claim 9, Marsan or Clauberg discloses the processing elements are operable to control the transfer of packet portions from the processing elements to an output device (an output device can be thought to collectively include the processing elements. Alternatively, Clauberg discloses from page 9, line 31 to page 10, line 3, of using a clock signal and an output of the processing element to control the mux).

20. Consider claim 59, Marsan or Clauberg discloses said output device is operable to collect processor data packets from the processing elements and to construct an outgoing data packet stream from collected processor data packets (Marsan, page 2, first indented paragraph, cells that are transferred to output interfaces, where they are

reassembled into variable-size IP datagrams; Clauberg, Figure 1, Mux 17 constructing output data stream 19).

21. Consider claim 60, Marson or Clauberg discloses said input device and said output device are part of an input/output system operable to transmit data to, and receive data from, the processing elements (each reference's input and output device can be collectively considered an input output system, which both transmits data to and receives data from the processing elements).

22. Consider claim 11, Clauberg discloses a plurality of such input devices and such output devices form part of a plurality of input/output systems, operable to transmit data to, and receive data from, the processing elements and adapted to support multiple input/output operations (Figure 1, each input or output to and from a specific processing element can be considered a separate input/output system).

23. Consider claim 40, Clauberg discloses a data processing architecture is implemented on a single integrated circuit (page 10, line 18, chip).

24. Consider claim 52, Marson discloses a processor comprising a data processing architecture (page 2, first indented paragraph, the overall router is a processor as it processes data).

25. Consider claim 16, Clauberg discloses a first plurality of parallel arrays of processing elements, and second plurality of hardware accelerator units (see Figure 1, processing elements 14.x and 15.x; these can also be considered hardware accelerator units, although Figure 4B also discloses of a processor and an AAL5 Segmentation and Reassembly unit which also serve as hardware accelerator units).

26. Consider claim 17, Clauberg discloses a plurality of parallel arrays of said processing elements, and a data input/output system which is operable to transfer data to and from the arrays of processing elements in turn (see Figure 1, processing elements 14.x and 15.x; these can also be considered hardware accelerator units; the IO structure includes the arrows to and from the processing elements).

27. Consider claim 44, Clauberg discloses the data processing architecture is implemented on a single integrated circuit (page 10, line 18, chip).

28. Consider claim 56, Marson discloses a processor comprising a data processing architecture (page 2, first indented paragraph, the overall router is a processor as it processes data).

29. Consider claim 20, Marson as modified by Clauberg discloses of a plurality of functional blocks chosen from: a single instruction multiple data (SIMD) processing element array, a data input device, a data output device, a hardware accelerator, a data

packet buffer and a bus structure for connecting the functional blocks to one another (see Figure 1 and the rejection of the independent claim).

30. Consider claim 21, Clauberg discloses the architecture is implemented on a single integrated circuit (page 10, line 18, chip).

31. Consider claim 32, Marson discloses a processor comprising an architecture or system (page 2, first indented paragraph, the overall router is a processor as it processes data).

32. Consider claim 63, Marsan as modified by Clauberg discloses that the number of processing elements is determined based on a bandwidth and an amount of required processing (it would have been obvious to one of ordinary skill in the art at the time of the invention that additional processing elements are added in order to increase processing capability; note, page 10, line 6, for example, which uses a variable to indicate the number of parallel paths).

33. Consider claim 64, Marsan as modified by Clauberg discloses wherein the size of the packet portions is determined based on a bandwidth and an amount of required processing (it would have been obvious to one of ordinary skill in the art at the time of the invention that the size of the packet portions has a direct correlation with the bandwidth of the router).

34. Claims 12-13, 19, 34-35, 38, 41, 53, and 61-62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan and Clauberg as applied to claims 1, 2, and 17 above, and further in view of Kejriwal et al. (Kejriwal) (US 6704794).

35. Consider claims 19, 34 and 38, Marsan and Clauberg do not explicitly disclose each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

On the other hand, Kejriwal discloses of a processing element which is operable to process data stored by that element in accordance with processing steps determined by the data concerned (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

36. Consider claim 12, Marsan and Clauberg do not explicitly disclose at least one processing element is operable to enter a standby mode of operation in dependence upon data received by that processing element.

On the other hand, Kejriwal discloses of a processing element which is operable to enter a standby mode of operation in dependence upon data received by that processing element (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

37. Consider claim 13, Clauberg discloses the at least one processing element is operable to enter the standby mode of operation when no data is received (see Figure 1, for example, no processing would occur when no data is inputted).

38. Consider claim 35, Kejriwal discloses each processing element is operable to process data stored by that element in accordance with processing steps determined by

the data concerned (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

39. Consider claim 41, Clauberg discloses the data processing architecture is implemented on a single integrated circuit (page 10, line 18, chip).

40. Consider claim 53, Marson discloses a processor comprising a data processing architecture (page 2, first indented paragraph, the overall router is a processor as it processes data).

41. Consider claim 61, Marsan and Clauberg do not explicitly disclose processing is only performed by processing elements containing packets or packet portions carrying a header.

On the other hand, Kejriwal discloses processing is only performed by processing elements containing whole packets or packet portions carrying a header (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

42. Consider claim 62, Marsan and Clauberg do not explicitly disclose processing is performed by multiple processing elements containing portions of a packet, in dependence on either data in the packet or information about the packet.

On the other hand, Kejriwal discloses processing is performed by multiple processing elements containing portions of a packet, in dependence on either data in the packet or information about the packet (col. 10, lines 27-43, for example, discloses how parsing packet header information from a cell is only done if there is packet header information in the cell; also see, for example, col. 11, lines 51-60).

Kejriwal's teaching of detecting whether a cell has packet header information, and only performing packet header operations if there is, enables the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kejriwal with the invention of Marsan and Clauberg in order to enable the correct conversion of cells into packets even in the event that multiple cells correspond to a single packet.

43. Claims 22, 46 and 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan and Clauberg as applied to claim 1 and 17 above, and further in view of ISSC95 (Evening Discussion Session).

44. Consider claims 22, 46, and 50, Marsan and Clauberg do not disclose that the architecture is implemented on a plurality of integrated circuits.

On the other hand, ISSC95 does disclose of architectures implemented on a plurality of integrated circuits (page 236, for example, multi-chip modules).

Multi-chip modules results in better yields, increased performance, and reduced cost, amongst other benefits (ISSC95, page 236, bottom two panelist statements, for example).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of ISSC95 with the invention of Marsan and Clauberg in order to gain better yields, increase performance, and reduce cost.

45. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marsan, Clauberg, and Kejriwal as applied to claim 12 above, and further in view of ISSC95 (Evening Discussion Session).

46. Consider claim 47, Marsan, Clauberg, and Kejriwal do not disclose that the data processing architecture is implemented on a plurality of integrated circuits.

On the other hand, ISSC95 does disclose of architectures implemented on a plurality of integrated circuits (page 236, for example, multi-chip modules).

Multi-chip modules results in better yields, increased performance, and reduced cost, amongst other benefits (ISSC95, page 236, bottom two panelist statements, for example).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of ISSC95 with the invention of Marsan and Clauberg in order to gain better yields, increase performance, and reduce cost.

Response to Arguments

47. Applicant argues on the paragraph spanning pages 10 and 11 that certain paragraphs of the specification support the concept that data transfer is initiated in response to a request from the processor, as claimed in claim 7. However, while data transfer may be controlled by the *processor*, the claim mandates that data transfer is controlled by the *processing elements*. See Figure 4, which shows the processing elements as merely a part of the overall processor; the thread sequence controller, for example, is part of the processor but not the processor elements. Therefore, it remains unclear as to nature of the control by the processing elements.

Applicant cites page 25, lines 5-6; however, this states that processors, and not processing elements, initiate datagram transfers. Applicant cites page 52, lines 3-18; however, while this may disclose how a processor operates via multithreading, this does not appear to disclose that the processing elements themselves control the data transfer (e.g. page 52, lines 4-5, disclose that each processor runs the same program). Applicant cites page 26, line 6 and onward, as disclosing that the distributor forwards

batches of packets to a processor in response to the request from the PEs; however, processing elements are not mentioned here. Applicant cites the paragraph spanning page 26, lines 12-20; however, while processors are disclosed here performing certain functions, processing elements are not.

Similarly, the specification does not appear to support the concept that data transfer to the output device is controlled by the processing elements specifically, as opposed to the processor in general.

48. Applicant argues from pages 13-16 the difference between the Marsan/Clauberg combination and the invention of the instant application. While each of these arguments will be addressed in turn below, the overarching summary is that, although there may be significant differences between the combination and the instant invention, each of these differences is not present in the claims.

49. Applicant argues on page 13 that the instant invention does not require that the size of data portions placed in the processing elements are equal or fixed in size. However, the instant claims do not contain any limitations which correlate to this facet of the instant invention.

50. Applicant informally argues on the bottom of page 13 regarding the benefits of the instant invention. However, the combination of Marsan and Clauberg still teaches the current claimed limitations.

51. Applicant argues on the top of page 14 that switching is not carried out in the instant invention, as opposed to Marsan, and thus one would be less likely to refer to Marsan as a starting point. However, it is first noted that the instant invention does appear to carry out switching, given its disclosure of a table lookup engine in the context of packet processing. Nevertheless, the presence of absence of a feature in the instant invention does not preclude the combination of a teaching of Clauberg to the invention of Marsan using a suitable motivation.

52. Applicant argues on page 14 of the differences between the instant invention and Clauberg. Applicant argues that because Clauberg distributes cells in a round-robin sequence, there is no distribution as such in the sense that the term is used in the instant invention. However, it would be improper to read the "distribute" limitation of the instant claims in a manner which correlates to the distribution as present in the instant specification. Consequently, Clauberg still teaches the claimed limitations.

53. Applicant argues in the paragraph spanning pages 14 and 15 that there is idle time in the processors of Clauberg, as opposed to the instant invention, because the instant invention makes effort to ensure that as many PEs as possible are active for as much time as possible. However, the steps and details regarding how this is done is absent from the current set of claims.

54. Applicant argues on page 15 that Clauberg does not disclose of the cells being distributed to the paths in dependence on the size of the incoming cells, and no dynamic distribution. However, the instant claims do not recite any limitations regarding distribution based on the size of an incoming cell, and it is possible to read "dynamic distribution" to mean that the path to which a cell is distributed is determined at the time of the receipt of the cell. To read "dynamic distribution" in a specific manner which is not mandated by the claims would be improper.

55. Applicant argues on page 15 that Clauberg is only capable of processing two cells at any one time, and is thus incapable of processing at least one packet at a time. However, it is first noted that processing "at least one packet at a time" includes the scenario of processing one packet at a time. Next, see Clauberg, page 3, line 12, which discloses of N parallel processing paths, and line 13, in which each path can comprise one or more processing units. In other words, it would be readily recognized that Clauberg is not limited to the specific example argued upon wherein only two cells are collectively in the processing paths at any given time. Moreover, it is noted that the processing of a specific cell of a packet still would meet the limitation that the packet is being processed. Therefore, in the two cell example, the claimed limitation would still be met when the last cell of one packet and the first cell of a second packet are collectively in the processing paths. Finally, the fact that Clauberg may teach a claimed limitation given a certain infrequent scenario does not preclude Clauberg from consequently teaching the claimed limitation; examiner recommends amending the

claim language in such a way to convey the inventiveness of the instant processor architecture. Applicant cites page 8, lines 18-23, of disclosing that entire packets are loaded into the processors. Although this is not claimed, it is noted that this occurs in Clauberg at least when the amount of cells in a packet are less than the amount of processing units in a processing paths. It is also noted that this limitation would be taught when a "processor" encompasses the, for example, FIFOs of page 7, line 25.

56. Applicant argues on page 16 that the amended limitation of "batches" overcomes the combination of Marsan in view of Clauberg. However, the aforementioned combination teaches the limitation in several ways. For example, the use of batch can simply refer to a set of data or jobs to be processed without human intervention (e.g. batch printing, in which a plurality of documents are all printed in a row rather an operator individually printing each document). In Marson, sets (in any arbitrary grouping) of incoming packets are "batches" as they will be split into cells consecutively. Similarly, in Clauberg, sets (in any arbitrary grouping) of cells are "batches" in that they will be processed consecutively. Note that "batches" in the claim can refer to either the data packets, or that which the data packets are distributed into.

Applicant cites pages 26, lines 6-11 and 19-30 as disclose a batch read mode; however, the details regarding this batch read mode are not claimed. Applicant cites page 59, lines 15-20; however, the details regarding this citation are not claimed and do not give further insight as to what exactly a "batch of packets" is aside from a group of packets. Applicant cites page 42, lines 24-30; however, the details regarding this

citation are not claimed and do not give further insight as to what constitutes a "batch". Applicant cites page 53, lines 8-17; however, the details regarding this citation are not claimed, and there is no indicate that "a batch of table look-up operations" have anything to do with the batches as used in the claim. Applicant cites page 54, line 27 through page 55, line 9; however, the details regarding this citation are not claimed, and do not give further insight as to what constitutes a batch. Applicant cites page 56, lines 4-14; however, the details regarding this citation are not claimed.

Applicant argues that the instant invention's operation through multithreading, where the PEs are programmable further distinguishes the instant invention from the prior art; however, these attributes are not claimed.

Conclusion

57. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183